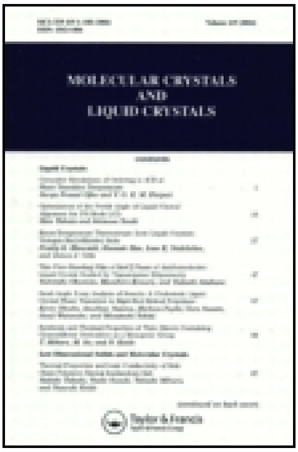


Molecular Crystals and Liquid Crystals
Publication details, including instructions for authors and subscription information:
http://www.tandfonline.com/loi/gmcl20

Characteristics of $CuInSe_2$ Superstrate Thin Film Solar Cell with Various Back Electrodes

Eun-Woo Lee [a], Bo-Sung Kim [b], Sang-Hwan Lee [c], Sang-Wook Park [d] & Yun-Su Lee [a]

[a] Advanced Display Advanced Display Manufacturing Research Center, Kyungpook National University, Daegu, Korea

[b] Mobile Display Research Center, Kyungpook National University, Daegu, 702-701, Korea

[c] Doosan Corporation, Electro-Materials, Development 1 Team, Gyeonggi-Do, Korea

[d] Department of Chemical Engineering and Technology, Yeungnam University, Gyeongsan, 712-749, Korea

Version of record first published: 30 Aug 2012.

Mol. Cryst. Liq. Cryst., Vol. 565: pp. 159–166, 2012

ISSN: 1542-1406 print/1563-5287 online
DOI: 10.1080/15421406.2012.693321

Characteristics of $CuInSe_2$ Superstrate Thin Film Solar Cell with Various Back Electrodes

EUN-WOO LEE,[1] BO-SUNG KIM,[2] SANG-HWAN LEE,[3] SANG-WOOK PARK,[4] AND YUN-SU LEE[1,*]

[1]Advanced Display Advanced Display Manufacturing Research Center, Kyungpook National University, Daegu, Korea
[2]Mobile Display Research Center, Kyungpook National University, Daegu 702-701, Korea
[3]Doosan Corporation, Electro-Materials, Development 1 Team, Gyeonggi-Do, Korea
[4]Department of Chemical Engineering and Technology, Yeungnam University, Gyeongsan 712-749, Korea

The maximum efficiency of $Cu(In_x,Ga_{1-x})Se_2$(CIS) superstrate thin film solar cell is smaller than that of CIS substrate thin film solar cell, but its device fabrication price is lower because the number of thin-film process is fewer. In addition, CIS absorber layer is fabricated through binary process to reduce the process temperature and processing price. In this study, CIS superstrate thin film solar cell was fabricated to reduce the device fabrication cost and CIS absorber layer was deposited by the binary process. By using Sodalime Glass (SLG), Al:ZnO and ITO were deposited on n-type transparent electrode layer in the upper part. CIS absorber was individually deposited by InSe(In_2Se_3) and CuSe in a binary type by using Molecular Beam Epitaxy (MBE). The deposited sample went through heat process, and then electrode was created to fabricate the device. In order to identify the structural and electrical characteristics of the various transparent electrodes, CIS absorber and CIS solar cell device, analysis was conducted by using X-ray Diffractometer(XRD, Bulk, PANalytical), Field Emission Scanning Electron Microscope (FE-SEM, S-4800, HITACHI), Inductively Coupled Plasma (ICP, ICPS-8100, Shimadzu), Secondary Ion Mass Spectrometry (SIMS, IMS 6F, CAMECA) and solar-simulator (AM1.5 g, 100 mW/cm_2).

Keywords Cu(In; Ga)Se_2; superstrate; thin film solar cell; binary; co-evaporation

Introduction

CIS thin film solar cell has higher efficiency, long-term stability and could fabricated at lower cost than crystalline silicon solar cell, and it can also be applied to flexible substrate including glass substrate [1]. The typical CIGS thin film solar cell is the substrate type and it is generally composed of sodalime glass(SLG)/back contact(Mo)/absorption layer(CIS)/buffer layer(CdS)/window layer(i-ZnO, Al:ZnO)/antireflection film(MgF2)/grid electrode(Al,Ni) [2,3]. In case of CIS substrate thin film solar cell, irradiation through SLG

*Address correspondence to Yun-Su Lee, Research Professor, Advanced Display Manufacturing Research Center, Kyungpook National University, 1370 Sangyeok-dong, Buk-gu, Daegu 702-701, Korea (ROK). Tel: (+82)53-950-7307; Fax: (+82)53-950-7313. E-mail: yunsulee@knu.ac.kr

substrate is not available but it is entered through the transparent electrode in the upper part, which requires a window layer with high transmittance transparent electrode. On the contrary, irradiation can be entered through SLG substrate in case of CIS Superstrate thin film solar cell, because CIS Superstrate thin film solar cell is composed of "Sodalime Glass(SLG)/window layer(TCO)/absorber layer(CIS)/electrode(Ag)" [4–6].

Currently, it has been reported that photovoltaic conversion efficiency of CIS thin film solar cell has reached 20% from the substrate architecture and 12.8% from the superstrate counterpart, showing that the efficiency is relatively lower than that of substrate-type cells. However, the device fabrication cost can be reduced because the number of processes to go through is fewer [7–9].

In addition to the cost reduction caused by the diminish of processes, it is also possible to minimize multi-layered thin film process, which has been the obstacle to the industrialization of CIS thin film solar cell. If this happens, then it can be applied to mass production of CIS thin film solar cell. However, an issue still remains even after the number of processes to fabricate Superstrate CIS thin film solar cell is diminished. It is that the process time and difficulty of process in the production of CIS absorber layer.

CIS absorber layer can be fabricated through 3-stage process, 1-stage process and binary process with thermal co-evaporator. It can also be fabricated through 2-step process which is sputtering Cu, In, Ga to make a precursor and proceeding with Se heat treatment [10–13].

From the point of efficiency, 3-stage process which uses thermal co-evaporator is the most desirable method, but it takes a long time to process and the cost of processing is high since it requires high consumption of materials and high processing temperature. In this regard, it is less likely that 3-stage process can be used for mass production.

From the point of efficiency, 3-stage process which uses thermal evaporator is the most desirable method, but it takes a long time to process and the cost of processing is high since it requires high consumption of materials and high processing temperature. In this regard, it is less likely that 3-stage process can be used for mass production. If both photovoltaic conversion efficiency and mass production are considered, binary process with thermal co-evaporation is the most proper method to use. Instead of depositing quaternary CIS, simple compounds of binary selenide such as CuSe and InSe are deposited and then Se heat treatment is done in order to fabricate CIS absorber layer. In this way, it can not only reduce the processing time but also lower the processing temperature to under 400°C. In this regard, this research employs CIS binary process to fabricate CIS superstrate thin film solar cell. SLG is deposited with both Al:ZnO(AZO) and ITO as transparent electrode and CIS, the absorber layer, is deposited with both InSe (or In2Se3) and CuSe as binary type by using thermal co-evaporator device. Then, heat process is done under Se environment to induce the reaction of $CuSe + InSe = CuInSe_2$ [13].

After CIS thin layer process is finished, electrode is created by using Ag paste. In order to identify the structural and electrical characteristics of various transparent electrodes, CIS absorber layer and CIS solar cell device, XRD, FE-SEM, ICP, SIMS and solar-simulator were used in this study.

Experimental

The structure and the production process of CIS Superstrate thin film solar cell is explained in Fig. 1. AZO or ITO (~800 nm,~30 nm) is deposited on after sodalime Glass (SLG) cleaning and window layer and then CIS absorber layer (~1.5 um) and Ag Electrode

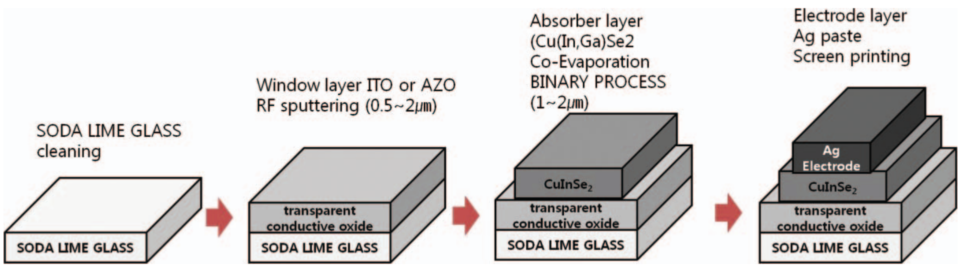


Figure 1. The fabrication processes and layer stack of CIS superstrate solar cell.

layer(~5 um) were proceeded in order. The size of the substrate that is used is 25 cm^2 and the thickness of the substrate is 0.7 or 1.2 mm.

In particular, thermal co-evaporator (YAS, substrate size: 100 mm × 100 mm) is used to fabricate CIS absorber layer since binary process is applied in this study.

The materials used in the fabrication of absorber layer are Cu, In, Ga and Se which is granular type with 99.999% of purity from Cerac. A halogen heater which can heat up to 800°C is used to heat the plate and effusion cell is used to heat the source.

The binary process used in this study is explained in Fig. 2. The order of process is InSe, CuSe and Se heat treatment. The temperature for each substrate is 150°C, 150°C and 400°C, respectively. The processing time for InSe, CuSe and Se heat treatment is 10 minutes, 15 minutes and 20 minutes, respectively. In this way, a sample was fabricated and then Ag electrode was formed through screen printing method.

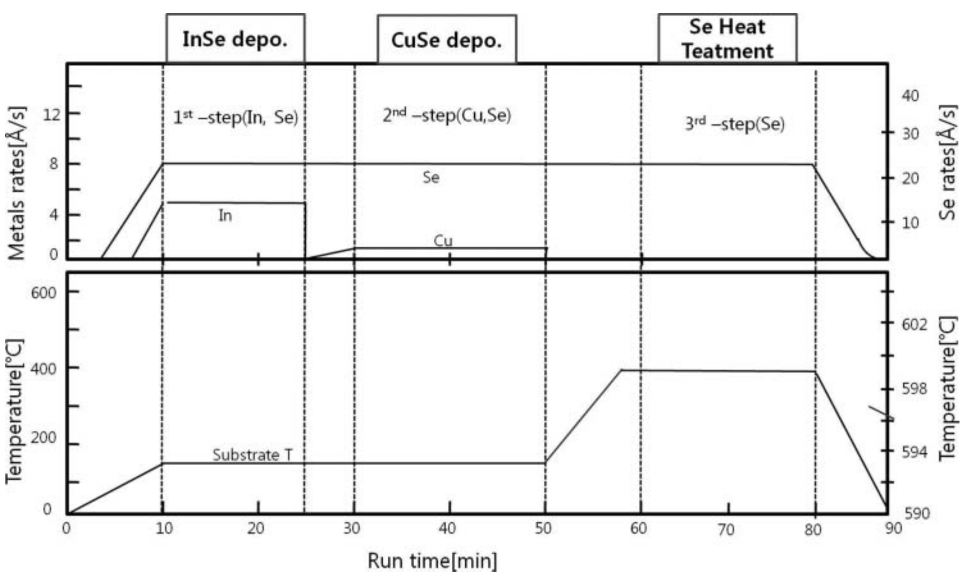


Figure 2. The variation of elemental fluxes and substrate temperature during the binary CIS deposition process.

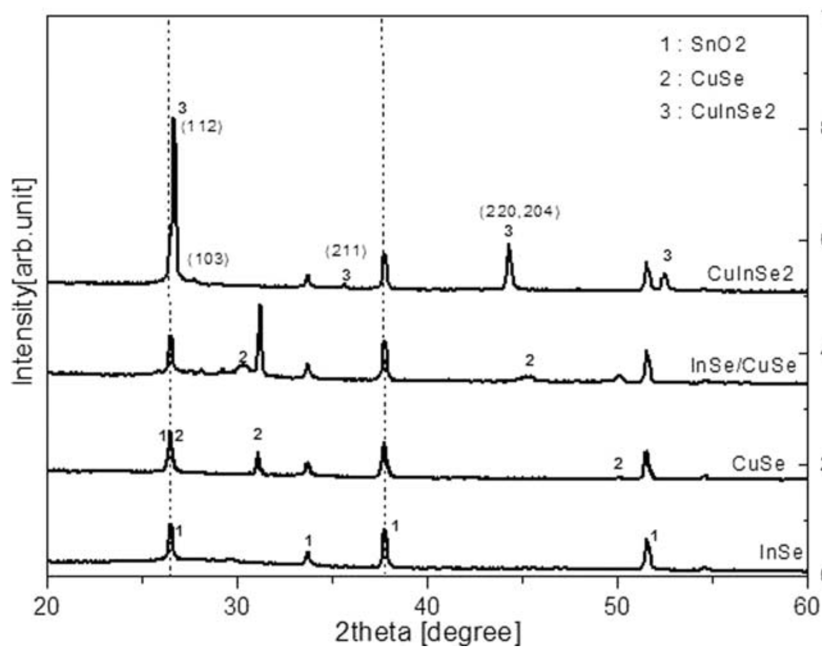


Figure 3. XRD patterns of the CIS binary samples.

Measurements

The characteristics of absorber layer and device was analyzed by using devices such as X-ray Diffractometer (XRD, PANalytical), Field Emission Scanning Electron Microscope (FE-SEM, S-4800, HITACHI), Inductively Coupled Plasma Atomic Emission Spectroscopy (ICP-AES, ICPS-8100, Shimatzu) and solar-simulator (AM1.5G, 100 mW/cm2).

Results and Discussion

The result of analysis on XRD is explained in Fig. 3, and it was analyzed for each stage of binary process.

Since the substrate temperature was remained at 150°C during InSe processing, it has the characteristics of amorphous material. In this regard, the phase cannot be identified with XRD.

However, CIS was formed after Se heat treatment. In this regard, it was likely that InSe was created as the first layer of the binary process.

Table 1. ICP measurement results.

	Mol Fraction				
CuInSe2	Cu	In	Se	Cu/In	Cu/Se
	0.1580	0.3604	0.4816	0.4384	0.3280

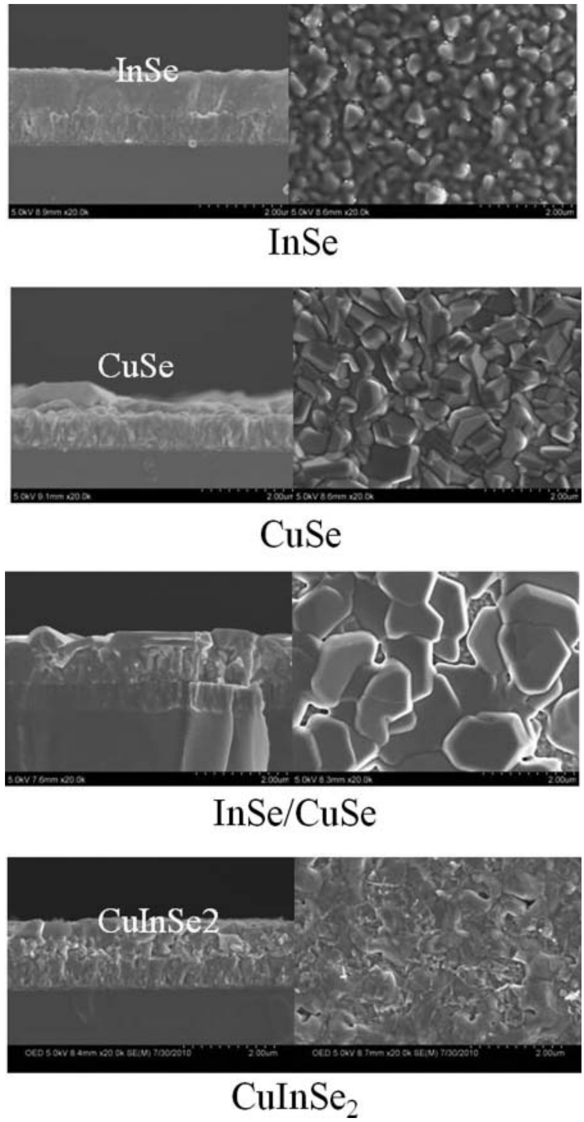


Figure 4. Cross-sectional and plan-view SEM images for the samples.

As a result of SEM, binary structure is identified in InSe/CuSe stack and the thickness of the layers is different; InSe 800 nm and CuSe 400 nm.

After heat treatment, SEM result showed other small crystals in addition to CIS. It could also be seen in SEM result explained in Fig. 4. Such small crystals were considered InSe which has relatively higher composition. In order to have the accurate result, ICP analysis was conducted.

ICP analysis result is shown in Table 1. The composition of Cu, In and Se was 0.158, 0.3604 and 0.4816, respectively. As the composition needed for the creation of CuInSe2 was Cu:In:Se = 0.158:0.158:0.316 (CIS), In and Se was left at the ratio of

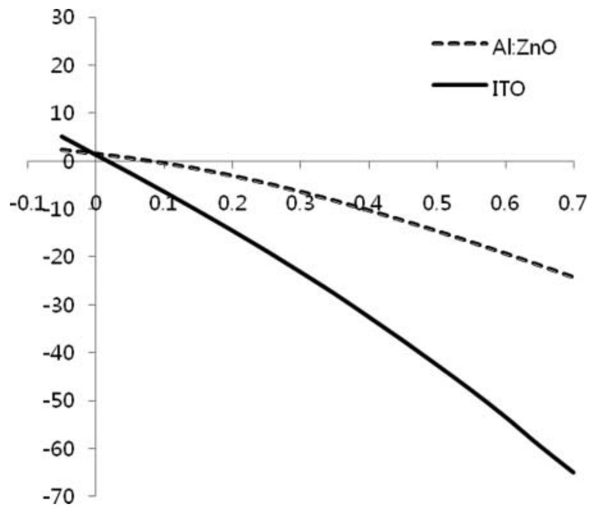


Figure 5. Current–voltage characteristics of CIS Superstrate solar cells measured under AM1.5 standard test condition.

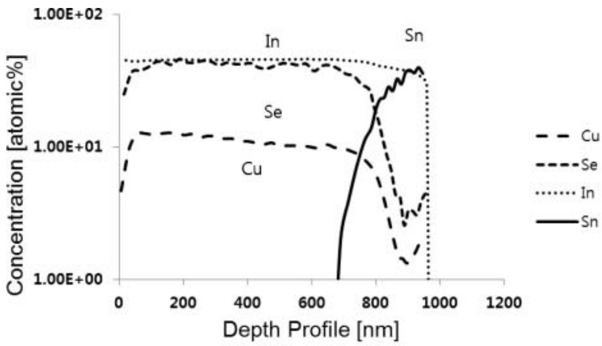
0.202:0.165. In this regard, the remaining In and Se were highly likely to exist as binary compound of InSe. It was possible to think of the possibility that the remaining In and Se exist as binary compound such as In_4Se_3 or In_2Se_3, but their XRD magnetic peak was not observed at all. In this regard, it was more likely that they remain as amorphous InSe.

Figure 5 shows the current-voltage curve that evaluates the solar cell device by using absorber layer shown in Fig. 4. Although a little difference was observed depending on transparent electrode (ITO or Al:ZnO), it was generally shown that leaky device with a very low shunt resistance is created.

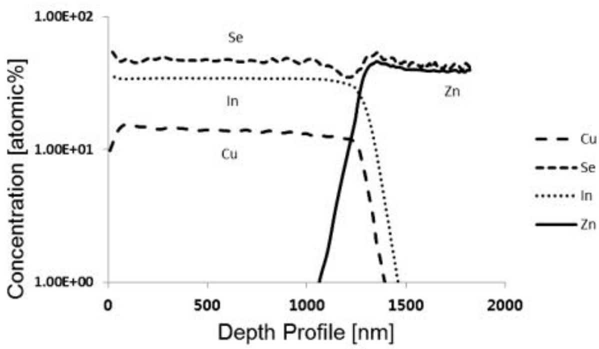
It is likely that leaky device is created because of InSe which exists in CIS crystal boundaries. In fact, InSe is a semiconductor with strong metallic characteristic [13]. If it exists though P-N junction, it can provide a shunt path. In this regard, InSe should be kept from remaining in the crystal boundaries to create Superstrate CIS solar cell device which can be normally operated. To do this, the thickness of binary selenide which comprises the stack and the post-treatment temperature should be precisely controlled. In particular, it is easier to eliminate the remaining InSe as the heat treatment temperature increases as InSe is known to be volatile.

However, if CIS formation temperature is high, another issue is brought about by the heat stability of transparent electrode. In particular, AZO which is widely used is known to loose initial physical characteristics after 400°C of heat treatment [8]. In this study, ITO with relatively high heat stability is compared with AZO to suggest the transparent electrode appropriate for Superstrate CIS solar cell.

Figure 7 is the result of the depth profile of a sample by using SIMS after AZO and ITO is respectively adopted as a transparent electrode and then through CIS formation process. The result shows a lot of Se diffuse after 400°C of heat process in the device using Al:ZnO transparent electrode.



a) CIS/ITO/SLG



b) CIS/Al:ZnO/SLG

Figure 6. SIMS measurement results.

Conclusions

In this study, CIS thin film with transparent electrode was deposited to Al:ZnO and ITO, respectively to fabricate the device in the order of InSe, CuSe and Se heat treatment by using binary process.

The result of structural characteristics shows issues in CIS composition. This is caused by excessive InSe and its electrical characteristics shows that p-n junction is not forged because shunt path is created in I-V curve.

The result of observation of the diffusion of heat treatment process under CIS binary process to window layer shows that a lot of Se diffuse in Al:ZnO transparent electrode even under 400°C of heat process. Accordingly, it is confirmed that the heat treatment appropriate for transparent electrode is needed and the CIS composition in CIS binary process is important.

References

[1] Mitchell, K. W., Eberspacher, C., Ermer, J., & Pier, D. (1989). *Proc. 20th IEEE Photovoltaic. Specialists Conf.*, pp. 1384–1389.
[2] Romeo, N., *et al.* (1986). *Proc. 7th E.C. Photovoltaic Solar Energy Conf.*, pp. 656–661.
[3] Nishitani, M., *et al.* (1994). *Proc. 1st World Conf. on Photovoltaic Energy*, pp. 222–225.

[4] Klenk, R., Mauch, R., Schäffler, R., Schmid, D., & Schock, H. W. (1991). "*Progress in CuGaSe2 based thin film solar cells*," in *Proceedings 22nd IEEE Photovoltaic Specialists Conference, Las Vegas*, pp. 1071–1076, IEEE.
[5] Negami, T., Nishitani, M., Wada, T., & Hirao, T. (1992). "Preparation of CuInSe2 films on CdS films for photovoltaic applications," *in Proceedings 11th European Photovoltaic Solar Energy Conference, Montreux,*. pp 783–786, Harwood Academic Publishers.
[6] Nakada, T., Okano, N., Tanaka, Y., Fukuda, H., & Kunioka, A. (1994). "Superstrate type CuInSe2 solar cells with chemically deposited CdS window layers," *in Proceedings 1st World Conference on Photovoltaic Energy Conversion, Hawaii*, pp. 95–98, IEEE.
[7] Repins, I., Contreras, M. A., Egaas, B., DeHart, C., Scharf, J., Perkins, C. L., To, B., & Noufi, R. (2008). *Progress in Photovoltaics: Research and Applications*, *16*, 235.
[8] Nakada, Tokio, Hirabayashi, Yutaka, Tokado, Takehito, Ohmori, Daiske, & Mise, Takahiro. (2004). *Solar Enetgy*, *77*, 739–747.
[9] Haug, F. J., Rudmann, D., Bilger, G., Zogg, H., & Tiwari, A. N. (2002). *Thin Solid Films*, *403–404*, 293–296
[10] Zhang, Li, He, Qing, Jiang, Wei-Long, LI, Chang-Jian, & Sun, Yun. (2008). *Chin.Phys.Left.*, *25*(2), 734
[11] Brummer, A., Honkimaki, V., Berwian, P., Probst, V., Palm, J., & Hock, R. (2003). *Thin Solid Films*, *437*, 297.
[12] Kim, W. K., Kim, S., Payzant, E. A., Speakman, S. A., Yoon, S., Kaczynski, R. M., Acher, R. D., Anderson, T. J., Crisalle, O. D., Li c, S.S., & Craciun, V. (2005). *Journal of Physics and Chemistry of Solids*, *66*, 1915–1919
[13] Kim, S., Kim, W. K., Payzant, E. A., Kaczynski, R. M., Acher, R. D.,Yoon, S., Anderson, T. J., Crisalle, O. D., Li, S. S., & Vac, J. (2005). *Sci. Technol. A*, *23* (2), 310–315.